Claims

The following is a copy of Applicant's claims that identifies language being added with underlining ("___") and language being deleted with strikethrough ("—"), as is applicable.

1. (Currently amended) A resistive cross-point array memory device, comprising:

a plurality of word lines extending in a first direction;

a plurality of bit lines extending in a second direction such that a plurality of cross points is formed at intersections between the word and bit lines; and

at least one memory element formed in at least one of the cross points, the memory element comprising ~~a first~~ an antifuse tunnel junction~~, the first tunnel junction comprising~~ having a bottom conductor, a top conductor, and a barrier layer adjacent the bottom conductor; ~~and~~

wherein the bottom conductor comprises a non-uniform upper surface.

2. (Original) The memory device of claim 1 wherein the bottom conductor further comprises one of the word lines and the top conductor comprises one of the bit lines.

3. (Canceled)

4. (Original) The memory device of claim 3 wherein the memory element further comprises an isolator element in series with the anti-fuse.

5. (Currently amended) The memory device of claim 4 wherein the isolator element is selected from the group consisting of a second tunnel junction, a magnetic tunnel junction, a diode, and a resistor.

6. (Original) The memory device of claim 3 wherein the average thickness of the barrier layer is between 10 and 30 angstroms.

7. (Original) The memory device of claim 3 wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

8. (Original) The memory device of claim 3 wherein the at least one memory element further comprises one of the memory elements formed at each cross point.

9. (Currently amended) An antifuse tunnel junction for use in a memory element, comprising:

a bottom conductor comprising an upper surface;

a top conductor; and

a barrier layer disposed between the bottom conductor and the top conductor; ~~and~~

wherein the barrier layer of the antifuse tunnel junction comprises a non-uniform surface.

10. (Original) The tunnel junction of claim 9 wherein the tunnel junction is an anti-fuse.

11. (Original) The tunnel junction of claim 10 wherein the average thickness of the barrier layer is between 10 and 30 angstroms.

12. (Original) The tunnel junction of claim 10 wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

13-14. (Canceled)

15. (Currently amended) A memory element comprising:

an anti-fuse comprising a bottom conductor, a top conductor, and a barrier layer of

non-uniform thickness therebetween; and

an isolator element in series with the first tunnel junction; ~~and~~

wherein the barrier layer has a dielectric breakdown voltage of between 2 and 3 volts.

16. (Currently amended) The memory element of claim 15 wherein the isolator element is selected from the group consisting of a second tunnel junction, a magnetic tunnel junction, a diode, and a resistor.